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Real-Time Comprehensive Condition Monitoring Technique for SiC MOSFET-Based Inverters in EV Applications

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Abstract

Reliable performance in various system operating modes is a substantial requirement in the new power electronics systems and applications. Wide Bandgap-based devices are favorable and appropriate choices for the new EV applications, specially inverter circuits which demands low loss and low parasitic performance in high voltage switching operation. A comprehensive condition monitoring system can have a major contribution in enhancing system reliability and solve the problem of reliability by observing the deterministic parameters in system failure and maintenance. In this paper, a comprehensive condition monitoring technique with a special focus on two major failure mechanisms of SiC MOSFETs is proposed. The results of evaluation tests show that broadening the condition monitoring vision into package-related as well as chip-related domains leads to having a more realistic and accurate monitoring data of the health of the switch during operation.

Keywords: , Chip-realted failure modes, Package-realted failure modes, Reliability, SiC MOSFETs;

1. Introduction

In automotive industry, depending on the ratings and the required operating conditions, various structures and materials of power semiconductors have been employed such as insulated-gate bipolar transistors (IGBTs), Silicon-based metal oxide semiconductor field-effect transistors (MOSFETs), Silicon Carbide (SiC)-based MOSFETs, and automotive-rated Thyristors Hazra et al. (2013), Schilling et al. (2012), Naghibi et al (2022). The existing

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semiconductor technology is mostly based on Silicon chips, which is so widespread and common since the invention of semiconductor technology. However, thriving of the new power electronics (PE) technologies such as Microgrids, Electric Vehicles, renewable energies, etc., demands some new features such as higher frequency operation, higher voltage and current ratings, less conduction power loss, and more temperature endurance of the employed components Schilling et al. (2012), Cao et al. (2020). The new power semiconductor technology, namely Wide Bandgap devices, can address majority of required device specifications in the new PE technologies Hazra et al. (2013), Naghibi et al. (2022), Schlechtingen (2013). Silicon Carbide and Gallium Nitride are the two materials that have been employed in WBG-based semiconductor devices as chip material successfully. Being capable to operate in higher temperature, higher voltage and current ratings, less conduction loss of the switch, etc. are making the WBG technology a favorable solution for the next generation PE technologies Lutz (2014). Some special considerations like thinner drift layer have led to have lower ON-state resistance, be capable of high frequency operation, and have a high temperature operation capability Gao et al. (2016), Cao et al. (2020), Nasab et al. (2019). In the Si-based devices, to manage large currents, parallel devices should be employed. But the current and voltage sharing problems in high temperature are impediments to have a reliable performance in these circuits Naghibi et al. (2022). However, Because of the smaller chip size (three times in comparison to Si-based devices) as well as having the capability of Multi-channel device configuration, WBG-based devices can operate in relatively high currents in a more reliable form Tsyokhla et al. (2019), Gonzalez-Hernando et al. (2019). This basically means that for inverter applications, although SiC MOSFETs can be a perfect choice for handing the power requirements, there are serious challenges and concerns regarding the reliable operation.

Reliable performance under harsh circuit and environmental distortions is a substantial prerequisite for any device to be used in inverter circuit of the new electric vehicle (EV) cars Gonzalez-Hernando et al. (2019). Although wide bandgap (WBG) devices can present the electrical and thermal characteristics required for a wide range of new PE technologies, the problem of the reliable performance is still a remaining concern. In aerospace, navy, EV, wind turbines, etc. as some of the new power electronics (PE) technologies, reliable performance is a basic requirement for thriving the technology. In traction applications, for example, lifetime of 20 years or more is required with the need for a high power cycling capability Gonzalez-Hernando et al. (2020). At the other end of the scale, industry standards of 68000 operating hours determine the lower limit of robustness for standard components Ceccarelli et al. (2019). Therefore, a solution for guaranteeing the reliable performance of the WBG technologies is required to enable this technology to be used in modern PE technologies. Condition Monitoring technique is a common solution for reliability assessment of the semiconductor devices. In Griffo et al. (2018), Baker et al. (2017), Naghibi et al. (2022), and Naghibi et al. (2021), some condition monitoring (CM) approaches for Si-based circuits are presented which are basically related to the applications in medium voltage level and the frequency range of below 20 kHz. These CM methodologies, however, cannot be perfectly applied to WBG-based circuits. In, an electrical parameters-based method is employed to monitor the junction temperature of the device as the main indicator of the device failure probability. It has been concluded that based on conduction resistance and power loss, the switch condition and the onset of the failure can be predicted Naghibi et al. (2022). However, it should be considered that in WBG devices, the power loss value is about three times smaller in comparison to that of Si devices. Considering the probable conduction noise and signal measurement error, a percentage change in this value, therefore, would be much challenging to be measured and interpreted. The same problem exists for the CM techniques using threshold voltage as the failure indicator.

In this paper, considering the aforementioned limitations in electrical parameters-based CM methodologies, a new CM technique for WBG-based circuits based on both failure modes of the SiC MOSFET is developed and evaluated. To overcome the problem of estimation and the small value change of electrical parameters in the CM techniques, the studies are concentrated on analyzing the device condition in different aspects. Both package-related and chip-related failures are induced in the switch and the proposed comprehensive CM technique is evaluated during both types of the degradation processes.

2. Package-Related Failure Modes of SiC Power MOSFETs

2.1. CM Precursor

Wire bond-related failure modes are the most common class of failure in package-related failure modes. For wire bond (WB)-related failure modes, ON-state Drain–Source voltage and body diode forward voltage were used as the health indicators in Gonzalez-Hernando et al. (2020) and Ceccarelli et al. (2019) respectively. Moreover, Junction-case thermal impedance is used as solder-related fatigue indicator Ni et al. (2020), Naghibi et al. (2021), and gate leakage current and forward voltage are used to detect body diode failure Ni et al. (2020). However, due to the smaller value of the abovementioned parameters in SiC MOSFETs in comparison to the ones of Si MOSFETs, adapting these parameters as CM precursors for SiC MOSFETs are erroneous.

In Naghibi et al. (2021), magnetic field of the wire bonds were used to detect any anomalies in the current distribution of the wire bonds in a wire bonded connection. Maxwell's equation suggests that for a specific amount of electrical current, which is passing from a single conductor with length of l, the surrounding magnetic flux density (B) is obtained as (1).

$$B = \frac{\mu_0 I_{WB}}{4\pi} \oint \frac{1}{r} d\theta \tag{1}$$

Based on the geometry of the conductor, the magnetic field of the surrounding area of the conductor can be characterized. Depending on the WB terminal type, e.g. WB connection of two adjacent chips, chip to baseplate, and baseplate to terminal, the geometry of the WB is altered. Despite minor differences in the structure of WBs, the overall WB geometry is modeled as a half hyperbola with one or two straight lines in the terminal areas (see Figure.1). The highest magnetic field is sensed at the center of the hyperbola-shaped wire, indicated by O in Figure.1. The total WB's magnetic flux density in 2D dimensions can be obtained by Biot–Savart law as (2).

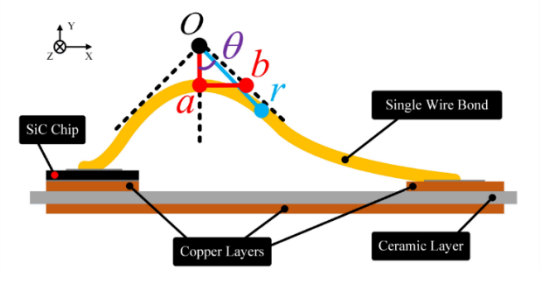


Fig. 1 A single WB geometry with the hyperbola shape structure

$$B = \frac{\mu_0 I}{2\pi a}\left[\left(\frac{1}{\xi}\right)\int_0^{\frac{\pi}{2}} \sqrt{1-\xi^2 sin^2\theta}\, d\theta + \left(\frac{\xi^2-1}{\xi}\right)\int_0^{\frac{\pi}{2}} \frac{1}{\sqrt{1-\xi^2 sin^2\theta}} d\theta\right] \tag{2}$$

Therefore, the highest sensed value of the originated magnetic field of a single WB at the center of the hyperbola is obtained as (2). This point is used to place magnetic sensors to measure the current of each wire bond (see Figure. 2). Any changes in the current value of a wire bond can be corresponded to wire bond-related failure.

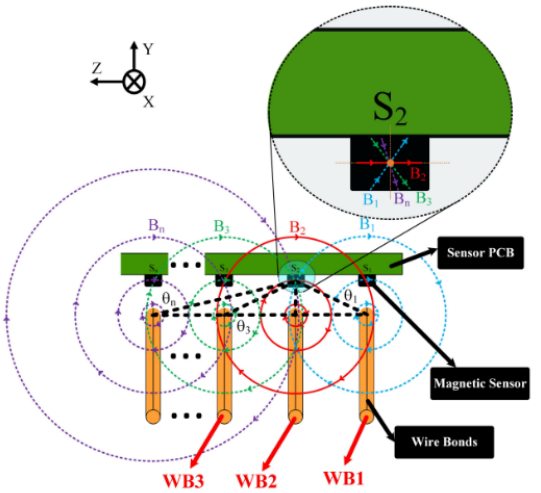


Fig. 2 Mutual effect of the adjacent WBs in the sensed magnetic field of WB2

2.2. Accelerated Lifetime Testing Method

In this section, the detection of the current distribution anomaly is validated experimentally. The proposed magnetic field-based CM technique is tested for the case study power module in a three phase inverter topology. Using a dedicated power cycling-based degradation set-up, we evaluate the developed CM technique. The case study switch (1200V/55A) is undergone 34k cycles. Monitoring is carried out using a sensor array with the external circuitry as shown in Figure. 3. Different scenarios were tested to cover different modes of wire bond failure. In Figure. 4, it is seen that in all the four considered scenarios, the proposed magnetic field based method can detect the onset of wire bond lift off or wire bond cracks.

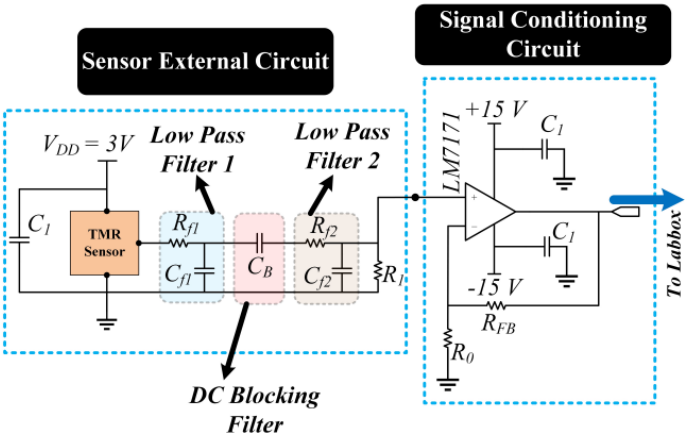


Fig. 3 External magnetic sensor circuitry and the signal conditioning section

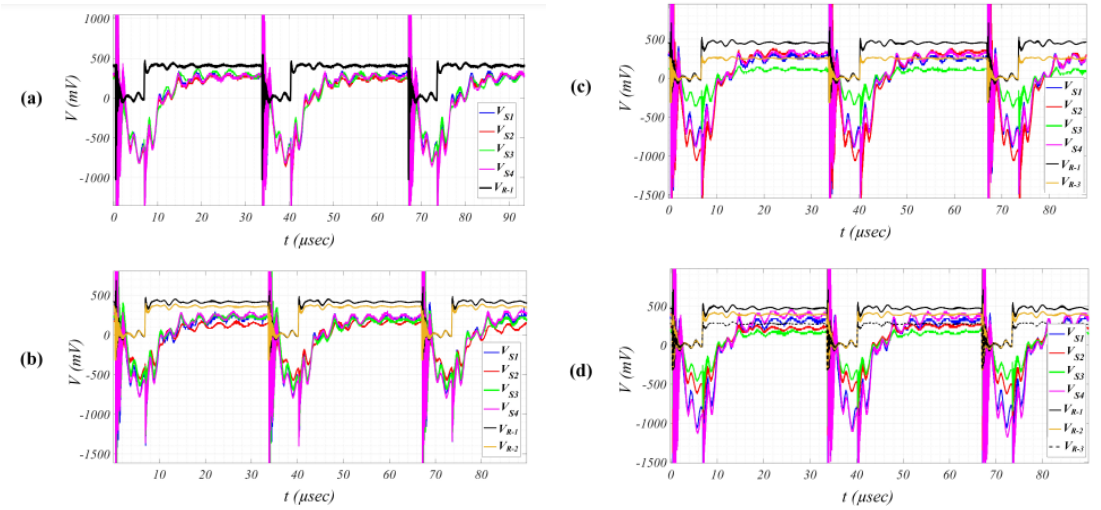


Fig. 4 Sensor array results in four different failure scenarios, (a) brand-new switch (b) 20% reduction in WB1 current conduction capability, (c) 80% reduction in WB3 current conduction capability, and (d) 20% reduction in WB1 and 80% reduction in WB3 current conduction capabilities

3. Chip-Related Failure Modes of SiC Power MOSFETs

3.1. CM Precursor

Different CM techniques are recently suggested to detect gate oxide degradation. V_{th}, drain leakage current, gate leakage current, Miller plateau voltage, gate-plateau time, and switch junction capacitance have been used as CM precursors in the literature Gonzalez-Hernando et al. (2020), Griffo et al. (2018), Baker et al. (2017), Naghibi et al. (2022), Ni et al. (2020), Naghibi et al. (2021). The employed failure precursors, which are generally adopted from the conventional Si-based MOSFETs, sometimes behave differently during the SiC MOSFET gate oxide degradation process in comparison to the ones of Si MOSFETs Lutz (2014). Therefore, specialized CM methods for the SiC MOSFETs should be developed. To achieve this, we have used a CM method using the device turn on transient changes due to gate oxide degradation.

Assuming V_{DS} falls linearly from V_{Bus} to 0V during switch turn-on process, device turn on time can be written as below.

$$t_{GP-on} = R_G C_{GD,avg} \frac{V_{DS}}{V_{Dr} - V_{GP}} \tag{3}$$

The device turn-on time strictly depends on the Miller plateau. Since V_{GP} increases due to gate oxide degradation, it can be concluded that t_{GP-on} also increases over the degradation process. As a result, $d(V_{DS})/dt$ in turn-on process of the device is decreased during the degradation. The variations of the device turn on transient is considered as the CM precursor. In Figure. 5, the effect of the gate oxide degradation on the rise time is shown during the device transitioning from brand-new to degraded conditions.

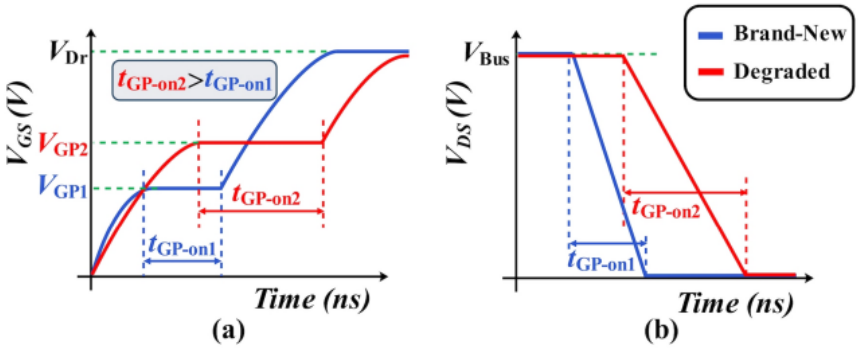


Fig.5 (a) Increment in V_{GP} and t_{GP} , and (b) decrement in d(V_{DS})/dt in turning-on process during degradation

3.2. CM Method and Implementation

V_{CM} is obtained based on a specific range of harmonic orders. In this regard, a well-tuned RLC filter is designed and placed on a voltage sample of V_{DS} as a band-pass filter. Defining i^{th} and j^{th} harmonic orders of V_S as the lower and higher cut-off frequency values of the chosen frequency envelope, the inductance and capacitance values of the RLC filter are obtained as below.

$$f_{cr} = \frac{f_s(i+j)}{2} = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{4}$$

In Figure. 6, the sampling circuit and the above-explained band-pass filter is shown. A relay is used to disconnect the circuit from the power terminals of the circuit to achieve more lifetime of the components. In control section, an optocoupler is used to achieve isolation between the measurement part and the signal part of the system. This facilitates the application of this method in practical implementations.

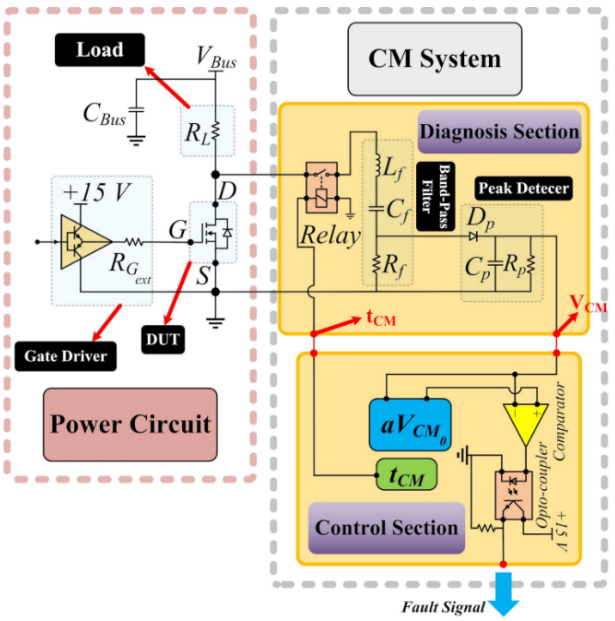


Figure. 6 Detailed view of the diagnosis and control sections of the proposed CM technique

4. Experimental Verification and Results

In Figure. 7, an overview of the implemented experimental set-up is shown. 3 phase SiC-based inverter is used as the circuit for the case study switch. In Figure. 8, the effect of device degradation is shown on V_{GS} and V_{DS} waveforms.

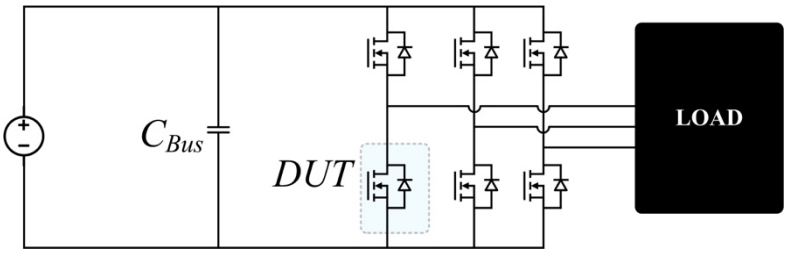
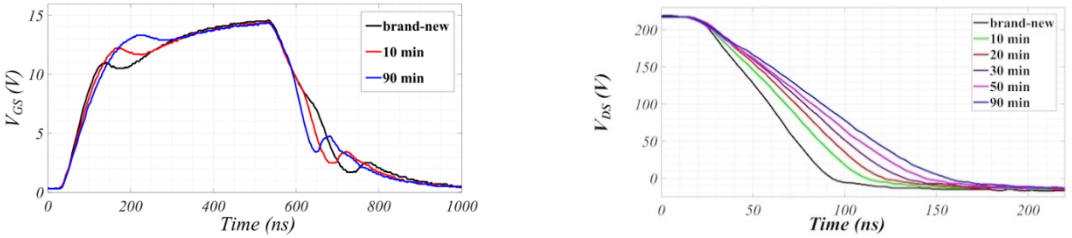


Fig. 7: three phase SiC inverter as the case study circuit



(a) (b)

Fig. 8: (a) V_{GS} and (b) V_{DS} waveforms changes during the device degradation

The proposed circuit in Figure. 6 is able to detect this change in the rise time. This means that the proposed CM technique is able to detect any chip-related failure mode.

5. Conclusion

Being focused on the two main failure modes of SiC MOSFETs, i.e. package-related and chip-related failure modes, a comprehensive condition monitoring technique was defined and evaluated in this paper. Current distribution anomaly detection was proposed as degradation indicator for wire bond degradation modes. Moreover, the changes in the turn-on transition behavior of the device was proposed and verified as a real-time failure precursor for gate oxide degradation. The experimental results of an inverter set-up showed that the proposed condition monitoring precursor is able to assess switch degradation level without having a galvanic connection to the power circuit. Real-time monitoring without switch operation interruption was also another achieved advantage in the proposed CM precursor.

References

S. Hazra, S. Madhusoodhanan, S. Bhattacharya, G. K. Moghaddam, and K. Hatua, 2013, “Design considerations and performance evaluation of 1200 v, 100 a sic mosfet based converter for high power density application,” in 2013 IEEE Energy Conversion Congress and Exposition, pp. 4278–4285.

O. Schilling, M. Schäfer, K. Mainka, M. Thoben, and F. Sauerland, 2012, “Power cycling testing and fe modelling focussed on al wire bond fatigue in high power igbt modules,” Microelectron. Reliab., vol. 52, pp. 2347–2352.

Naghibi J, Mohsenzade S, Mehran K, Foster MP, 2022, “Gate oxide degradation condition monitoring technique for high-frequency applications of silicon carbide power MOSFETs” IEEE Transactions on Power Electronics, 38(1):1079-91.

B. Gao, F. Yang, M. Chen, M. Dong, P. Duan, and U. Irfan, 2016, “A temperature spectrum density distribution based condition evaluation method and application in igbt,” Applied Thermal Engineering, vol. 106, pp. 1440–1457.

J. Lutz, 2014, “Packaging and reliability of power modules”, 8th International Conference on Integrated Power Electronics Systems, pp. 1–8, VDE.

H. Cao, P. Ning, X. Wen, T. Yuan, and H. Li, 2020, “An electrothermal model for igbt based on finite differential method,” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 673–684.

Naghibi J, Mohsenzade S, Mehran K, Foster MP, 2022, “Evaluation of Drain-Source Voltage in Switch Transient Time Intervals as Gate Oxide Degradation Precursor of SiC Power MOSFETs” 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), pp. 1-9, IEEE.

M. Schlechtingen, 2013, “A Global Condition Monitoring System for Wind Turbines”, PhD thesis, Technical University of Denmark (DTU).

J. N. Nasab, A. Hadizade, S. Mohsenzade, M. Zarghany, and S. Kaboli, 2019, “A marx-based generator with adjustable fwhm using a controllable magnetic switch,” IEEE Transactions on Dielectrics and Electrical Insulation, vol. 26, no. 2, pp. 324–331.

I. Tsyokhla, A. Griffo, and J. Wang, 2019, “Online condition monitoring for diagnosis and prognosis of insulation degradation of inverter-fed machines,” IEEE Transactions on Industrial Electronics, vol. 66, no. 10, pp. 8126–8135.

F. Gonzalez-Hernando, J. San-Sebastian, A. Garcia-Bediaga, M. Arias, F. Iannuzzo, and F. Blaabjerg, 2019, “Wearout condition monitoring of igbt and mosfet power modules in inverter operation,” IEEE Transactions on Industry Applications, vol. 55, no. 6, pp. 6184–6192.

F. Gonzalez-Hernando, J. San-Sebastian, M. Arias, A. Rujas, and F. Iannuzzo, 2020, “Discontinuous pwm for online condition monitoring of sic power modules,” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 323–330.

L. Ceccarelli, R. M. Kotecha, A. S. Bahman, F. Iannuzzo, and H. A. Mantooth, 2019, “Mission-profile-based lifetime prediction for a sic mosfet power module using a multi-step condition-mapping simulation strategy,” IEEE Transactions on Power Electronics, vol. 34, no. 10, pp. 9698–9708.

A. Griffo, J. Wang, K. Colombage, and T. Kamel, 2018, “Real-time measurement of temperature sensitive electrical parameters in sic power mosfets,” IEEE Transactions on Industrial Electronics, vol. 65, no. 3, pp. 2663–2671.

N. Baker, H. Luo, and F. Iannuzzo, 2017, “Simultaneous on-state voltage and bond-wire resistance monitoring of silicon carbide mosfets,” Energies, vol. 10, no. 3, p. 384.

J. Naghibi, S. Mohsenzade, K. Mehran and M. P. Foster, 2022, "Package-related degradation condition monitoring of SiC power MOSFETs using current distribution anomaly detection," 11th International Conference on Power Electronics, Machines and Drives (PEMD), Hybrid Conference, Newcastle, UK, pp. 728-732, doi: 10.1049/icp.2022.1145.

J. Naghibi, S. Mohsenzade, S. Iqbal, K. Mehran and M. P. Foster, 2021, "On the Effect of SiC Power MOSFET Gate Oxide Degradation in High Frequency Phase Leg-Based Applications," IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2022, pp. 1-6, doi: 10.1109/ECCE50734.2022.9947441.

Z. Ni, X. Lyu, O. P. Yadav, B. N. Singh, S. Zheng and D. Cao, 2020, "Overview of Real-Time Lifetime Prediction and Extension for SiC Power Converters," in IEEE Transactions on Power Electronics, vol. 35, no. 8, pp. 7765-7794, doi: 10.1109/TPEL.2019.2962503.

Naghibi J, Mehran K, Foster MP, 2021, “High-frequency non-invasive magnetic field-based condition monitoring of sic power mosfet modules”, Energies. 14(20):6720.