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# Improved design of a DC-DC converter in residential solar photovoltaic system

**Mantas Darameičikas[1], Firdaus Muhammad-Sukki[2], Siti Hawa Abu-Bakar[3], Nazmi Sellami[4], Nurul Aini Bani[5], Mohd Nabil Muhtazaruddin[6], Abdullahi Abubakar Mas'ud[7], Jorge Alfredo Ardila-Rey[8]**

[1,2,4] School of Engineering, Robert Gordon University, United Kingdom
[3,5,6] Universiti Kuala Lumpur British Malaysian Institute, Malaysia
[6] UTM Razak School of Engineering and Advanced Technology, Universiti Teknologi Malaysia, Malaysia
[7] Department of Electrical and Electronics Engineering, Jubail Industrial College Saudi Arabia
[8] Department of Electrical Engineering, Universidad Técnica Federico Santa María, Chile

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**ABSTRACT**

With growing demand in renewable energy, solar photovoltaic (PV) technology is becoming more popular. A number of research has been carried out to increase the efficiency of the PV system. One of them is improving the Switch Mode Power Supplies (SMPS) performance to ensure maximum solar energy extraction. This paper looks at buck type SMPS suitability for use in solar PV installed in residential houses. The main issues that affect the response from the output are identified. The work will utilise the LT SPICE software to carry out the simulation. The primary objective of the study is to design an improved converter controller which is more robust and is able to maintain constant output. The emphasis is on good efficiency, stability and low output voltage ripple. This could be achieved by using the current mode control (CMC) techniques – an alternative design to the voltage mode control technique (VMC). Results obtained via simulations reveal strong evidence of CMC superiority over the VMC.



***Corresponding Author:***

Mantas Darameičikas,
School of Engineering,
Robert Gordon University,
Garthdee Road, Aberdeen, AB10 7GJ, Scotland, United Kingdom.
Email: mdarameicikas@yahoo.co.uk

## 1. INTRODUCTION

With constantly depleting conventional energy sources, changes in climate and increasing pollution levels, an alternative such as renewable energy sources became popular. Over the last 200 years energy demand was met from non-renewable sources such as coal, natural gas and oil. With continuous rising in energy demand, the world's oil, natural gas and coal resources will be depleted by the end of this century. Currently the European Union aims to reduce greenhouse gas emissions by 95% by year 2050 [1]. One of the solutions is to increase the use of renewable energy technology.

Solar photovoltaic (PV) has seen a tremendous growth in the past 20 years [2, 3]. Continuous cost reduction and incentives from government are some factors that enable the uptake of this technology [2, 4–11]. Additionally, it also has a cheaper installation cost and a lower maintenance cost when compared with other renewable sources [4], [12–19]. In the United Kingdom (UK) for example, the solar PV systems range in size from small stand-alone systems to large scale, grid-connected power systems [1]. With over 80% of public support and 8 GW of solar PV being deployed in country, solar power is earning its popularity. Implementation climbs at the rate of 150,000 homes in country every year. The trend is expected

to result in 4 million UK households running on solar energy by 2020 [20]. It is believed by many experts that by 2030 the world's electrical energy demand can be provided by renewable energy sources alone [21].

Despite a growing trend in terms of installation, globally, solar PV only contributed to a small fraction of energy production – approximately 2.1% of the world's electricity demand [2]. In various parts of the world, especially in developing countries, the installation cost of solar PV systems is higher than conventional power sources [5, 7], although it has no fuel cost [22]. Many studies have been conducted to increase the efficiency of existing solar cells, which can be considered as moderate at the moment. Besides that, other researchers have also tried to maximise the energy capture by optimising the conversion efficiency of the PV system. A DC-DC converter is one of the key components in the system, where high efficiency and low output voltage ripple are crucial parameters that need to be satisfies at converter design stage. This work will focus on design and simulation of DC-DC converters to be used in residential solar PV system.

Previously, the authors have presented the voltage mode control (VMC) as a potential solution [23], and the test closely replicating the method demonstrated in [24]. From the simulations [23], it was found that the transient response was critically damped and it was also observed that there is no overshoot. The output voltage ripple was significantly reduced from 80 mV to 56 mV, which was achieved without implementing additional capacitor [23]. The VMC technique also reduced the settling time by 0.6 s [23]. By using the bode plot analysis, the compensator circuit was evaluated and the parameters of the main system stability were identified and recorded, achieving an infinite gain and a phase margin of 89$^o$ [23]. However, the developed model in [23] is still considered as having a slow transient response. This paper presents an alternative to the VMC technique - by using the current mode control (CMC) technique with the objectives of reducing the transient response time.

## 2. METHODOLOGY

To carry out the simulation in LT SPICE, it is important to determine the correct value of the components needed in the CMC circuit configuration. These values will be determine using specific equations which are presented in Section 2.1. Once these values are determines, the simulations are carried out and this is explained in Section 3.

### 2.1. Current mode control

The current mode control (CMC) offers an improvement to VMC. An additional inner loop is used as seen in Figure 1. The inner loop controls the inductor current and is faster than the outer voltage loop [25]. Using VMC, inductance varies with input voltage. Duty cycle decreases as input raises causing a higher effective inductance, making the loop responses slower. After the input or load, transient inductor in VMC needs several more cycles to reach a new steady state level. Using CMC the inductance is not part of the plant transfer function. This eliminates the issue occurring in VMC. A two pole second order filter is reduced to a single pole first order filter. Such improvement allows for simpler compensation networks. Ramp voltage is generated by sensing the inductor current. This is usually accomplished by using current sensing amplifier seen in Figure 2. To avoid losses, the sensing resistor has to be of low value. Typically in range of tens of milliohms. The sensed current is then converted to proportional voltage ramp and applied to the comparator input.

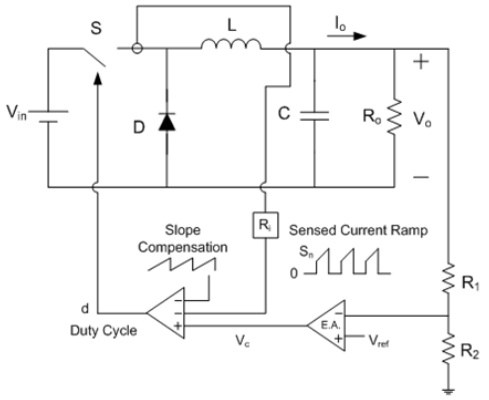


Figure 1. Current mode control [26]

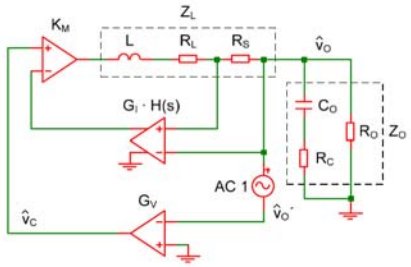


Figure 2. Simplified loop representation [25]

The type of CMC implemented here is the peak current mode control (Figure 3). The rising slope of the inductor current is compared with error amplifier voltage Vc. Once inductor current exceeds the Vc the duty cycle pulse becomes zero. The main switch is then off until the next clock pulse arrives.

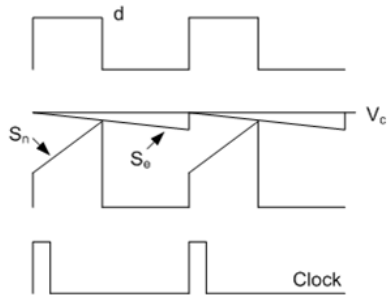


Figure 3. Peak current mode control modulator waveforms [26]

Design of the current loop can be perceived by using simpified diagram in Figure 2. The plant transfer fucntion in this case becomes:

$$G_{vd}(s) = \frac{R_L}{R_M} \times \frac{1+\frac{s}{\omega_{ESR}}}{\left(1+\frac{s}{\omega_o}\right)\times\left(1+\frac{s}{Q\times\omega_n}+\frac{s^2}{\omega_n}\right)} = \frac{R_L}{R_M} \times \frac{1+\frac{s}{\omega_{ESR}}}{\left(1+\frac{s}{\omega_o}\right)} \quad 1)$$

where $R_M$ is transresistance. It is the pulse width modulation (PWM) voltage gain divided by sensed inductor current.

Effective series resistance (ESR) zero is given by:

$$f_z = \frac{1}{2\pi C_o R_{ESR}} = 2\ kHz \quad 2)$$

The output load pole is expressed as:

$$f_p = \frac{1}{2\pi C_o R_L} = 67\ kHz \quad 3)$$

where $R_L$ is the load resistance.

As there is only one pole and a zero, type two compenstator seen in Figure 4 can be used. $R_f$ is chosen to be 240 kΩ to achieve good value of the closed loop gain.

$$G_{EA} = 20\log\left(\frac{R_f}{R_1}\right) = 9\ dB \quad 4)$$

The desired crossover frequency is 10 kHz. The error amplifier zero is placed a decade below this frequency.

$$f_{ZEA} = \frac{1}{2\pi R_f C_f} = 1\ kHz \quad 5)$$

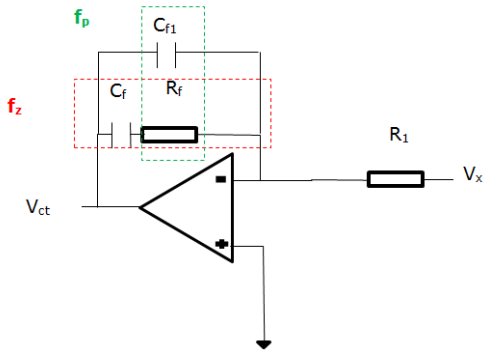


Figure 4. CMC Error amplifier with type 2 compensation

This can be rearranged for $C_f$ as

$$C_f = \frac{1}{2\pi R_f f_{ZEA}} \quad 6)$$

$$f_z = \frac{1}{2\pi R_f C_{f1}} = 2\ kHz \quad 7)$$

This allows $C_{fl}$ to be found

$$C_{f1} = \frac{1}{2\pi R_f f_z} \quad 8)$$

By applying Equations (1)-(8) above, the error amplifier component values can be obtained and these are summarised in Table 1.

Table 1 CMC error amplifier component values

| Component | Value |
|---|---|
| R1 | 85 kΩ |
| $R_f$ | 240 kΩ |
| $C_f$ | 680 pF |
| $C_{fl}$ | 390 pF |

## 3. RESULTS AND DISCUSSION

Simulation model of CMC can be seen in Figure 5. Corresponding transient response with this control is shown in Figure 6. Output voltage still produces critically damped response as with VMC. Initial model has suffered from high output voltage ripple. A third parallel capacitance branch was added as control measure, indicated by orange dotted lines. This helped to smooth output ripple to acceptable level, below 100 mV. Moreover, despite the use of type 2 compensation initially, desired performance was not achieved. An amendment was made by including additional compensator zero. This was performed by adding capacitor in parallel with voltage divider network resistor R1.This is demonstrated in Figure 5 with red dotted lines.

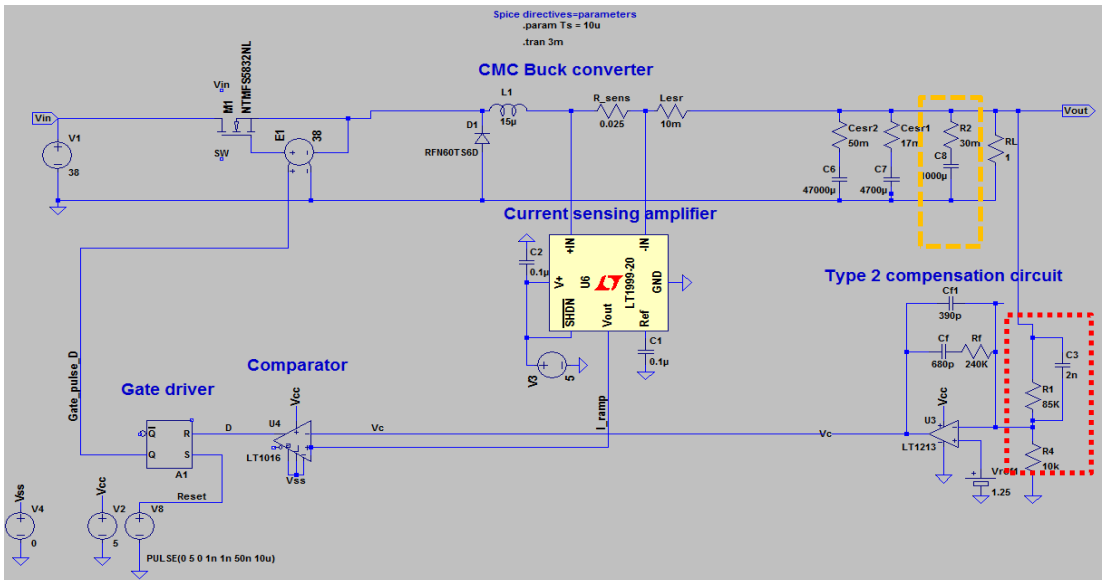


Figure 5. LT spice model of CMC buck converter

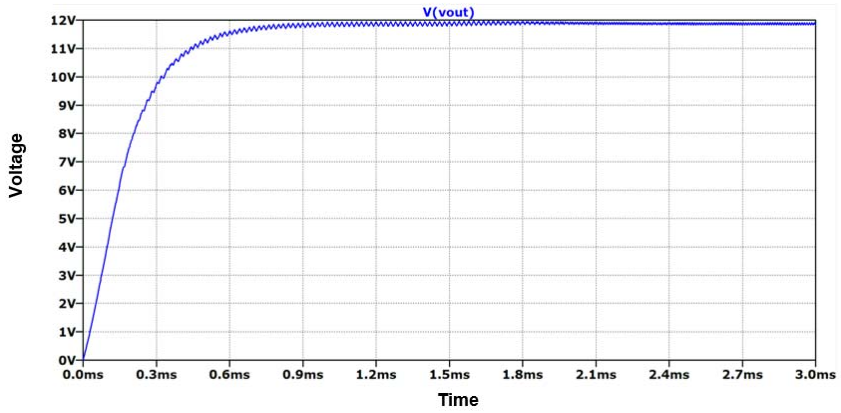


Figure 6. Transient response of closed loop CMC buck converter [1]

Converter ability to respond to supply and load variations is tested. Tables 2 and 3 show response to changes at output and input side respectively. It was observed that the converter responds to changes at load. Also, constant desired output voltage is maintained. There is a decrease of 0.3 s in settling time compared to results in [23]. Furthermore a slight increase of 4 mV in output voltage ripple is evident.

Table 2. CMC buck converter response to load variation

| $V_{in}$ = 38V | | | | |
|---|---|---|---|---|
| $R_{Load}$ (Ω) | Overshoot (%) | Tsett (ms) | Vripple (mV) | VOut (V) |
| 0.5 | 0 | 1.2 | 60 | 12 |
| 1 | 0 | 1.2 | 60 | 12 |
| 3 | 0 | 1.2 | 60 | 12 |
| 5 | 0 | 1.2 | 60 | 12 |
| 6 | 0 | 1.2 | 60 | 12 |
| 8 | 0 | 1.2 | 60 | 12 |
| 20 | 0 | 1.2 | 60 | 12 |
| 100 | 0 | 1.2 | 60 | 12 |

Table 3. CMC buck converter response to input variation

| $V_{in}$(V) | $R_{Load}$ (Ω) | Overshoot (%) | $T_{sett}$(ms) | $V_{ripple}$(mV) | $V_{out}$(V) |
|---|---|---|---|---|---|
| 10 | 1 | 0 | 18 | 0 | 9.5 |
| 15 | 1 | 0 | 4.0 | 120 | 12 |
| 20 | 1 | 0 | 1.2 | 120 | 12 |
| 25 | 1 | 0 | 1.2 | 100 | 12 |
| 30 | 1 | 0 | 1.2 | 60 | 12 |
| 35 | 1 | 0 | 1.2 | 60 | 12 |

Constant output for voltages of 15 V and above is maintained. However, device settling time with 10 V input is greatly increased; the settling time is 9 times greater when compared to results found in [23]. No overshoot exists at this input level. For all other input voltage levels, the settling time is reduced to 1.2 s. Output voltage ripple is higher with lower input voltages. Ripple then decreases with increase in input voltage. This is the opposite for VMC technique. Figure 7 illustrates the compensator stability parameters. Result is as expected for type two compensation. The lower gain than with VMC can be identified. Phase margin is lower by 9º compared to previous model in [23] and gain is lower by 30 dB. Similar differences are also acknowledged in [27].

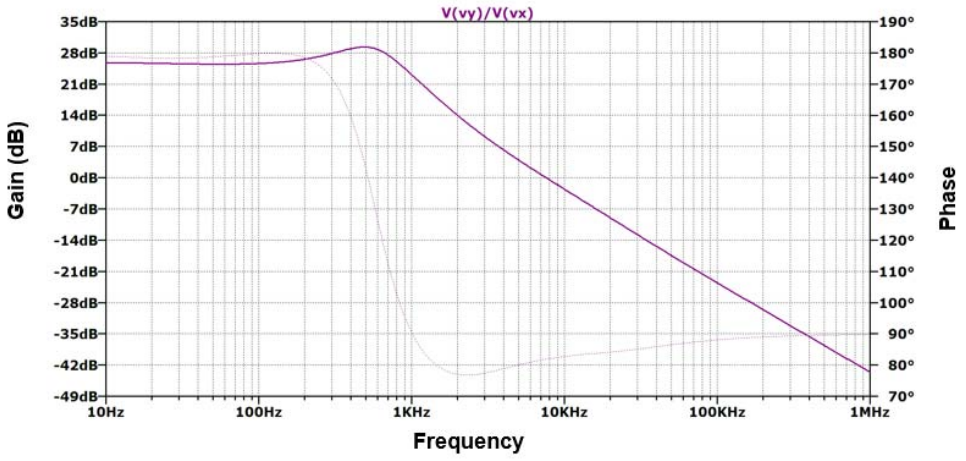


Figure 7. CMC loop gain bode plot indicating stability

## 4. CONCLUSION

This paper investigated an improved design of DC-DC converter for residential solar PV application. The CMC is proposed to deliver improved performance than the VMC technique. This is achieved by modifying VMC converter and introducing additional current sensing loop. Modified type 2 compensation circuit is used to provide the desired performance. The CMC circuit was simulated using the LT SPICE software. Reduced transient response time has emerged as a key advantage of this improved convertor design where a settling time is reduced to 1.2 s regardless of changes in input and output sides. For variations in supply voltage converter, CMC demonstrated a reversed situation compared to the VMC case. High output voltage ripple appeared at lower input voltage levels and reduced with increasing supply voltage. CMC, just as VMC, also benefited from critically damped transient response.

Some alterations to initial design were required to deliver satisfying performance. The need for smoothing capacitor to reduce output voltage ripple arises. Even with capacitor being added, results demonstrate a slight increase of 4 mV in output ripple for load changes, compared to VMC. Effective control of output ripple is essential to prevent reduction in PV panel ouput. Design of compensator circuit also requires some reconsideration. Supplementary zero is needed to achieve acceptable result. Stability does not appear to be greatly affected compared to VMC. Phase margin is lower by 9˚ and gain is lower by 30 dB.

The whole two loop compensation scheme design is more complex than VMC. Nevertheless, the proposed control technique delivers improved performance demonstrating its superiority over the VMC. Thus it is a suitable solution for solar PV applications.

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